HEART RATE COMPUTATION IMPLEMENTED ON FIELD PROGRAMMABLE GATE ARRAY BOARD

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Abstract

Heart rate is the most basic information of heart activities. This paper aims to describe a possible real time system to detect electrocardiogram (ECG) signal, count the R-R interval of the ECG signal, and compute the heart rate. This project is implemented successfully using field programmable gate array (FPGA) board.

Keywords: Heart rate, ECG, FPGA.

1. INTRODUCTION

The electrocardiogram (ECG) is a technique of recording bioelectric currents generated by the heart. This technique produces an ECG signal, which is a biological signal that shows the electrical activities of the heart as shown in Fig. 1. This signal is used to observe some basic information of the heart condition and determine whether the heart monitored is suffering from any abnormalities.

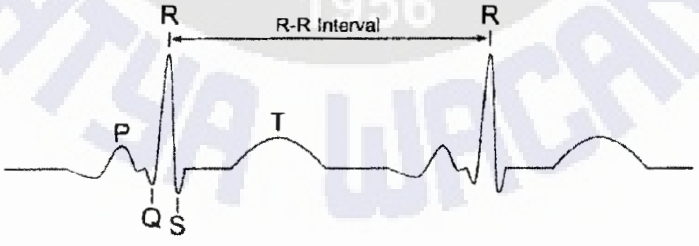


Fig. 1. ECG signal

The most basic information monitored from ECG signal is heart rate. Heart rate can be computed using the R-R interval of the ECG signal. This paper aims to make a real time system to detect the ECG signal, count the R-R interval, and compute the heart rate. This research uses very-high-speed-integrated-circuit hardware description language

(VHDL) on an Altera cyclone school boy field programmable gate array (FPGA) board to compute the heart rate.

The block diagram of the system is illustrated in Fig. 2. In the ECG block, a circuit is designed to obtain the ECG signal from the human body. The output of this ECG block is the input to the FPGA board. The processes to be done within the FPGA board include the analog to digital conversion (ADC) of the ECG signal, the algorithm to measure the heart rate, as well as the digital to analog conversion (DAC) of the signal which marks the R points. An oscilloscope is used to display the output.

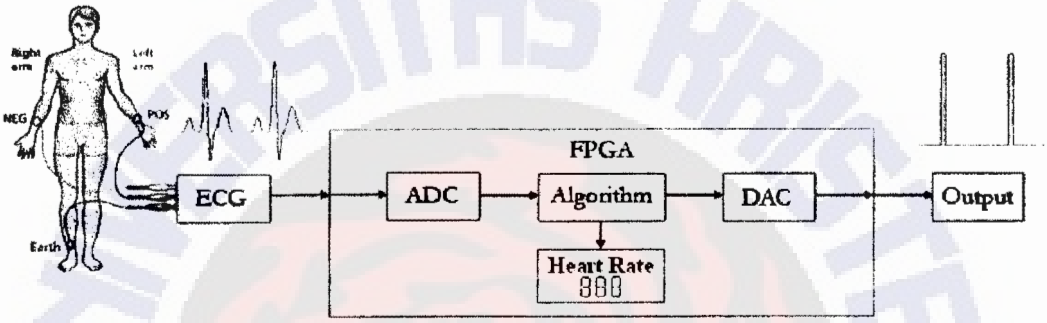


Fig. 2. The block diagram of the system

2. ECG CIRCUIT

In general, biological signals are very small. An ECG signal is approximately 0.1 to 6 mV [1]. Therefore amplification is needed in order to monitor them better. Fig. 3 and Fig. 4 show the block diagram and the circuit diagram of an ECG amplifier. The system starts with taking the signal from the body by connecting self-adhesive electrodes to significant part of the body. Then, the signal is amplified using an instrumentation amplifier. After that, it goes through a band pass filter that eliminates noise of the input signal.

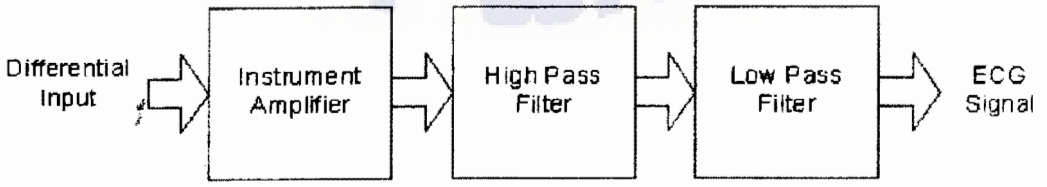


Fig. 3. ECG amplifier block diagram

An instrumentation amplifier is used to attenuate common biological signal from the positive and negative inputs produced by not-heart body organs and amplify the difference between the inputs produced by heart. An instrumentation amplifier having a high common mode rejection ratio (CMRR) is needed for this application. The instrumentation amplifier circuit used in the system is shown in Fig. 5. The gain can be computed using Eq. 1. To control the CMRR, a variable resistance was placed between the reference and instrumentation amplifier [1].

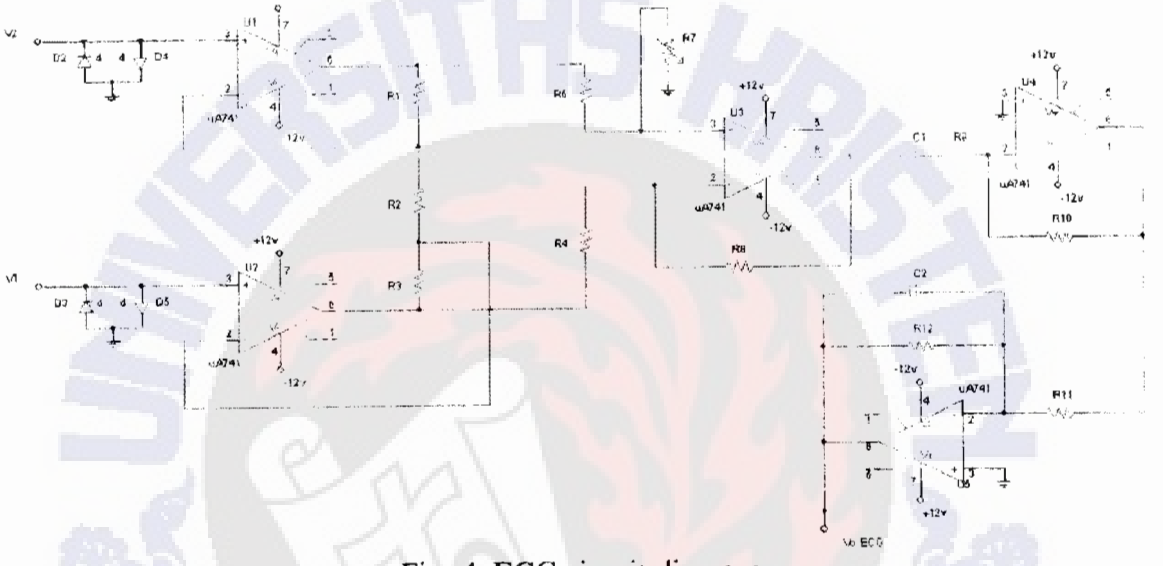


Fig. 4. ECG circuit diagram

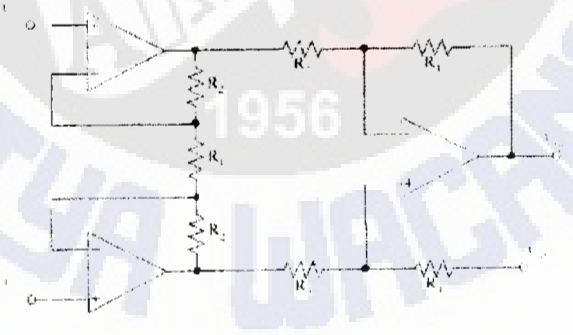


Fig. 5. Instrumentation amplifier circuit diagram

$$V_{out} - V_{Ref} = \frac{R_4}{R_3}\left(1 + 2\frac{R_2}{R_1}\right)(v_1 - v_2) \qquad (1)$$

The band pass filter is made out of cascaded high and low pass filter. Since the frequency range of an ECG signal is from 0.5 to 100 Hz [1], the cutoff frequency of the

high pass filter is 0.5 Hz and the cutoff frequency of the low pass filter is 100 Hz. Fig. 6 and Fig. 7 show the connection of a simple first order inverting active high pass filter with a unity gain and a simple first order inverting active low pass filter with a unity gain [2]. Eq. 2 is used to compute for the resistance and capacitance value of the high pass and low pass filter.

$$R_1 = \frac{a_1}{2\pi f_c C_1} \tag{2}$$

where a_1 is the gain, R_1 is the resistance value, C_1 is the capacitance value, and f_c is the cutoff frequency. Since the filters are unity gain, the value of R_2 is equal to that of R_1 [2].

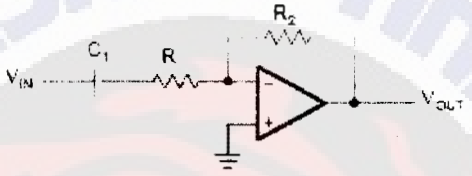


Fig. 6. First order inverting active high pass filter

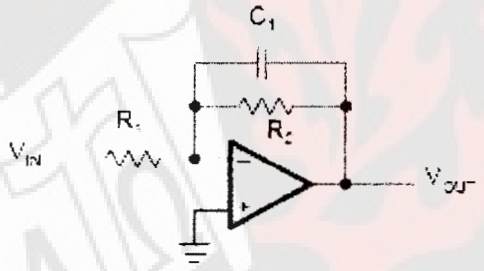


Fig. 7. First order inverting active low pass filter

Fig. 8 shows the ECG signal generated from the ECG amplifier. Since the ECG signal of each person differ in strength, the amplifier is made such that the gain of the instrumentation amplifier may be adjusted to conform to the required signal strength by the FPGA module.

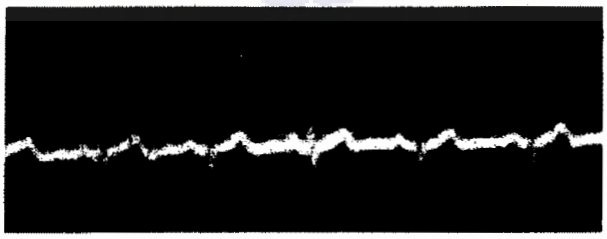


Fig. 8. Resulted ECG signal

III. SYSTEM IMPLEMENTED ON FPGA

The output of the ECG circuit is then feed to a FPGA board. The digital algorithm implemented on the FPGA aims to point out the R points and calculate the real time heart rate. The approach implemented on the FPGA board starts with a moving average filter to remove the high frequency noise. Then, it followed by R point finding and the heart rate calculation. The detail digital algorithm is shown at Fig. 9.

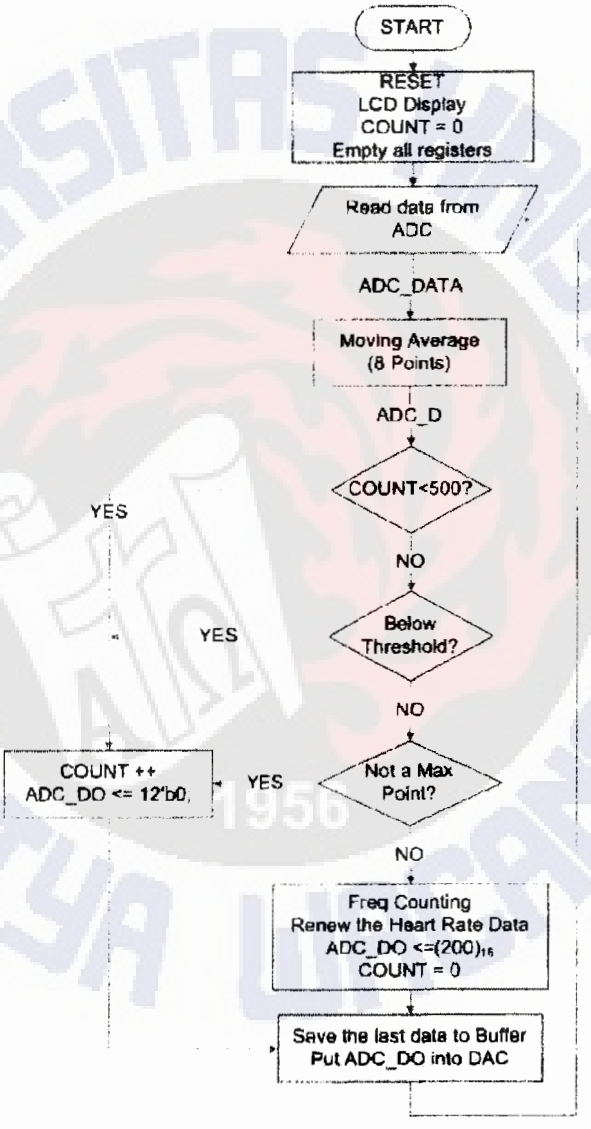


Fig. 9. Digital system flowchart

First, the system clears all register and makes a welcome display on the liquid crystal display (LCD). Then, the digital system takes data from the ADC with a sampling

frequency 2 kHz and conducts an eight point moving average filtering to remove the high frequency noise. Theoretically, the moving average filtering is made by adding the last 8 data, then dividing the result by 8. However, a divider is avoided to make the system simple. Therefore, we used three right shifts to replace the divider. The moving average system is explained in Fig. 10.

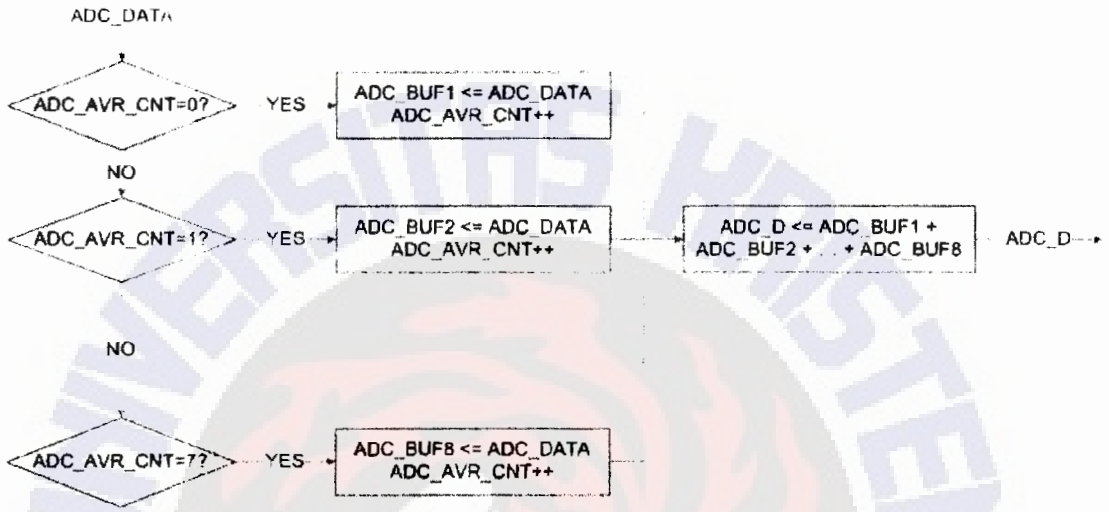


Fig. 10. Moving average flowchart

After conducting moving average filtering, the algorithm wants to locate the R points. In the implemented system, a point is considered as an R point if the point is not excessively close to the previous R point, the point is above certain threshold, and the point is a maximum point.

The interval between two R points is called by R-R interval. This R-R interval is counted with the help of variable 'count'. After conducting a moving average, the system waits until variable 'count' is higher than 500 samples. This approach is implemented to avoid calculation based on excessively close maximum points and to make the overall system faster. Even though the overall ECG information ranged from 0.5 to 100 Hz [1], the human heartbeat rarely goes above 4 Hz or 240 bpm. Therefore, we can expect that there is no new R point in ECG signal within ¼ second (500 samples) after the previous R point. Note that if we expect to count a heartbeat faster than 240 bpm, the constant 500 should be lowered.

If the count is already higher than 500 samples, the system checks if the data concerned is above the threshold. After the concerned data is above certain point, the system checks whether it is a maximum point. The applied method for conducting a maximum point calculation is explained in Fig. 11. A point is considered as a maximum point if this point is the highest point among its 24 neighbor samples. The common approach used to find a maximum point is called gradient method. However, the approach applied is has a little different with the gradient method. The gradient method takes the centre point of Fig. 12a as a maximum point, but do not take the centre point of Fig. 12b as a maximum point. The applied method takes both centre points of Fig. 12a and Fig. 12b as a maximum point. The applied method was chosen to minimize the effect of the high frequency noise.

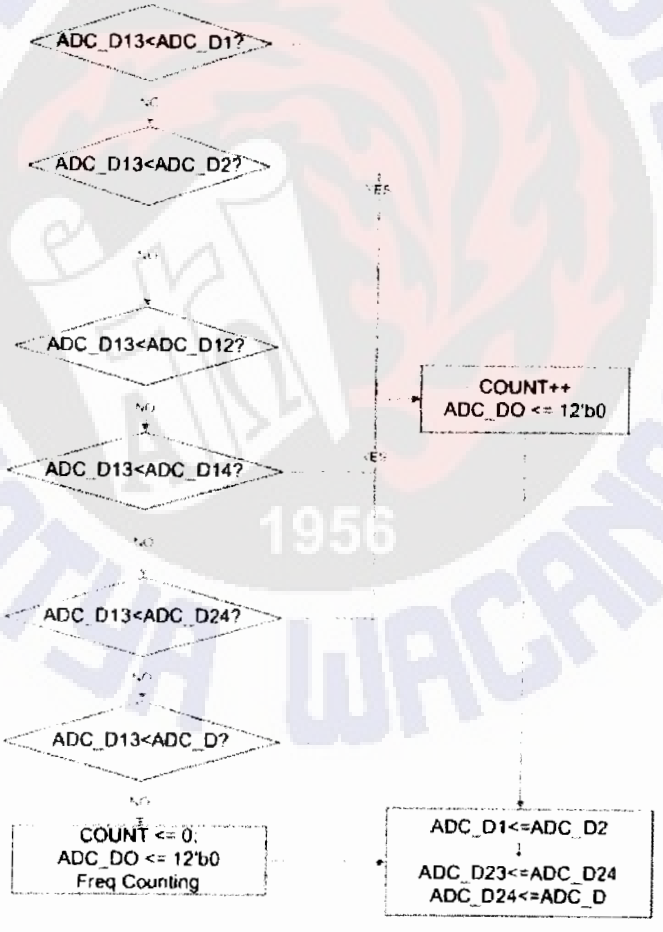
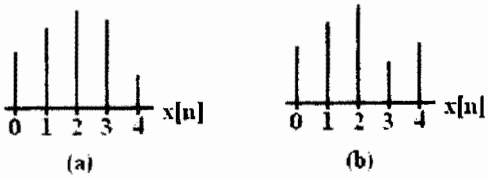


Fig. 11. Maximum point flowchart



Gradient Method:
x[1] - x[0] > 0
x[2] - x[3] > 0
x[3] - x[2] < 0
x[4] - x[3] < 0

Applied Method:
x[0] < x[2]
x[1] < x[2]
x[3] < x[2]
x[4] < x[2]

Fig. 12. Two different maximum point methods

After a point is considered as a maximum point, the system puts some value at the DAC output and calculates the heart rate. This DAC output is used to see whether all R points are point out correctly. The heart rate calculation is based on the variable 'count' which indicates the R-R interval. Given that the ADC sampling frequency is 2 kHz, by using this variable we can count the heart rate (per minutes) using the following equation:

$$\text{Heart Rate (/min)} = \frac{\text{Sampling Freq (/sec)} \times 60}{\text{Count}} = \frac{120000}{\text{Count}} \quad (3)$$

For displaying the computed heart rate into seven-segment display, first, we need to determine the hundreds, tenth, and ones value of the heart rate. The method for conducting the frequency-hundreds is explained in Fig. 13, the analogous method is used for the tenth and ones. The results are sent to the seven-segment display, which is controlled by a finite state machine (FSM). After the computation is done, the variable count starts from zero again, for the next R-R interval. Then, the data buffer is renewed for the next moving average and maximum point calculation.

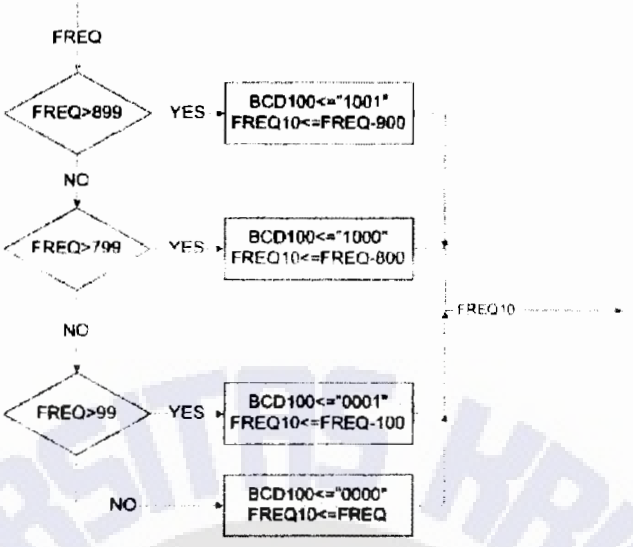


Fig. 13. Frequency-hundreds approach

IV. RESULTS AND DISCUSSION

To test the algorithm on the FPGA, we used sine waves from the signal generator as the FPGA input. First, we used a 2 Hz signal. The result can be seen at Fig. 14 where output of the DAC pointed out the maximum points correctly and the seven-segment display showed the heart rate 125 bpm.

Fig. 14. 2 Hz input, display: 125

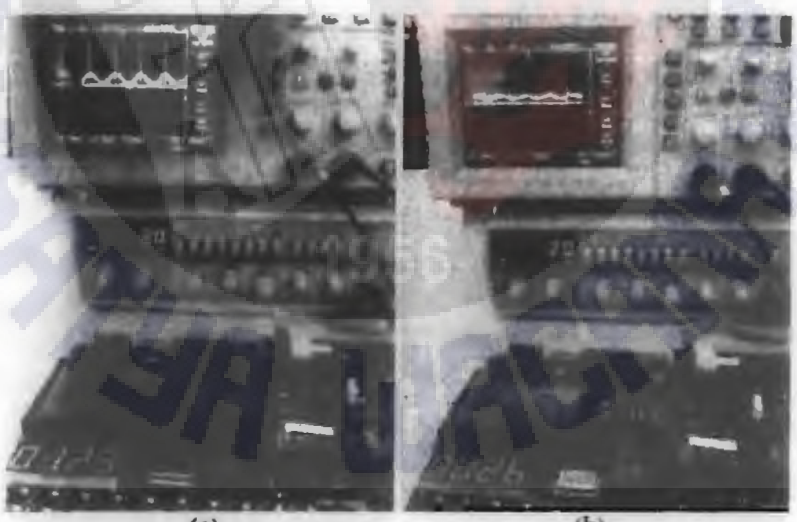
The highest heart rate that this system can handle is 4 Hz or 240 bpm. The results can be seen at Fig. 15. This limitation is due to the approach that the minimum R-R interval is 500 samples. Not all maximum-point of a signal between 4 Hz and 100 Hz can

be detected, as shown in Fig. 15b. Therefore, the heart rate display is lower than the actual frequency. For a signal above 100 Hz, no maximum point is detected as shown in Fig. 15c. This happened because the actual maximum points are not the highest among its 24 neighbor samples.

(a) (b) (c)

Fig. 15. (a) 4 Hz input, display: 231 (b) 10 Hz input, display: 194 (c) 100 Hz input

In the implemented system, a signal is consider as a maximum point if the signal magnitude is higher than 80 mV as shown in Fig. 16a. If the signal is lower than 80 mV, no maximum point is detected as shown in Fig. 16b.



(a) (b)

Fig. 16. (a) 2 Hz, 100 mV input, display: 123 (b) 2 Hz, 80 mV input, display: 26

To test the overall system, we connect the ECG circuit to human and the result is shown in Fig. 17. As shown in the figure, all R points are detected correctly. The display shown in the seven-segment display indicates the real time heart rate.

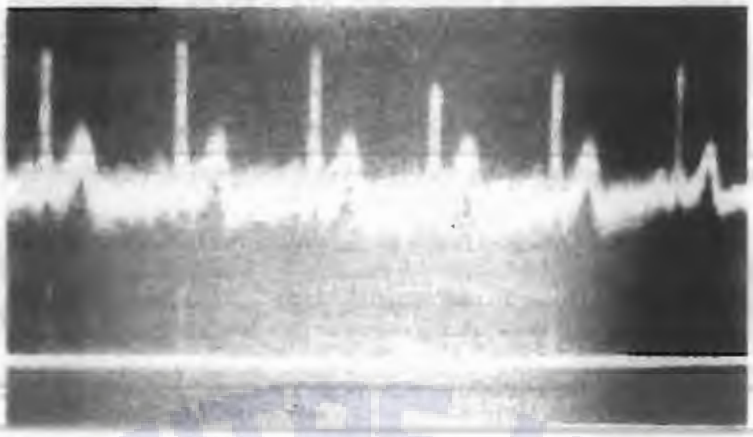


Fig. 17. Detected R points of a ECG signal

This paper described one possible method to detect electrocardiogram (ECG) signal, count the R-R interval of the ECG signal, and compute the heart rate. In the future, an algorithm to detect the other points and give some information regarding the heart rate variability (HRV) will complete this research.

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